Amendments to the Specification:

Please replace the paragraph starting on line 31 of page 4 with the following amended paragraph:

Unlike conventional DRAMs, the cache system 50 also includes two SRAM arrays 80, 84 that are each coupled to the sense amplifier/write driver circuit 64 to access data in the DRAM array 60. The SRAM arrays 80, 84 are also coupled to the refresh controller 78. The refresh controller 78 receives addresses from the address decoder 52, and it applies addressing and control signals to the row driver 54. Although SRAM arrays 80, 84 are shown in Figure 2 for use as auxiliary memory devices, it will be understood that other types of memory devices that need not be refreshed may also be used as auxiliary memory devices.